Notice of Allowability	Application No.	Applicant(s)	
	10/064,098	ALLEN ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed 06/11/2002*.

2. ☒ The allowed claim(s) is/are *1-27*.

3. ☒ The drawings filed on *10/28/2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

A. M. Thompson
Primary Examiner
Technology Center 2800

DETAILED ACTION

1. This office action is in response to the Application 10/064,098 filed 06/11/2002.

2. Claims 1-27 are pending in the Application.

Allowable Subject Matter

3. Claims 1-27 allowed. The following is an examiner's statement of reasons for allowance: in a method of reducing shorts in an integrated circuit having cells, the prior art does not include a step of creating a cloned cell by removing a via identified as faulty from an original cell.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bracha et al. (US Patent 5,798,937) discloses the redundant via software scans for places in close proximity to the critical via where redundant vias can be placed electrically in parallel to the critical via; in another form, the redundant via software searches for areas that will allow the contact opening of the critical via to be extended or widened to improve the reliability of the critical via, wherein significant increase of integrated circuit yield has been observed using the redundant via methods taught herein, but lacks evaluating an original cell containing a faulty via to determine if

a redundant via exists for the faulty via; and removing the faulty via from the original cell to create a cloned cell. Papadopoulou et al. (US Patent 6,247,853) discloses providing an efficient method to compute critical area and critical regions for via blocks by characterizing the critical region of a via shape for several geometries as a function of the defect size, wherein in certain geometries (including the Euclidean), the critical region of one via shape grows uniformly as the defect radius increases; based on these characterizations, providing an incremental algorithm to compute critical area for via blocks which is valid for several geometries; wherein the incremental computation is efficient because it takes advantage of the hierarchical structure typical of VLSI designs, in which repeated geometric patterns are represented by cells consisting of shapes and transforms on usages of those cells; but lacks evaluating an original cell containing a faulty via to determine if a redundant via exists for the faulty via; and removing the faulty via from the original cell to create a cloned cell. Regan (US Patent Application Publication 2003/0084418) discloses a process for modifying the design of integrated circuits including the steps of mapping cells of an old circuit against a library of new cells and replacing at least some of the old cells with new cells having the same logical function as the old cells, while maintaining the electrical connections between those cells, wherein the geometry of the electrical connections between the cells is then re-routed, but lacks evaluating an original cell containing a faulty via to determine if a redundant via exists for the faulty via; and removing the faulty via from the original cell to create a cloned cell. Anderson et al. (US Patent 6,415,421) discloses an integrated verification and manufacturability tool provides more efficient verification of integrated

device designs than verification using several different verification tools; the integrated verification and manufacturability includes a hierarchical database to store shared design data accessed by multiple verification tool components (e.g., layout versus schematic, design rule check, optical process correction, phase shift mask assignment and machine language conversion), wherein the hierarchical representation provided by modified database provides several performance advantages, but lacks identifying faulty vias as ones having a chance of shorting that is above a predetermined threshold; evaluating an original cell containing a faulty via to determine if a redundant via exists for the faulty via; and removing the faulty via from the original cell to create a cloned cell.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

A.M. Thompson
Primary Examiner
Technology Center Z800

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center Z800